34. A semiconductor device, comprising:

a first gate electrode on a substrate;

a second gate electrode on the substrate, the second gate electrode adjacent to and spaced apart from the first gate electrode;

a pair of first gate spacers at respective sides of the first gate electrode;

a pair of second gate spacers at respective sides of the second gate electrode;

a first interlayer insulating layer on the substrate, the first interlayer insulating layer between one of the pair of first gate spacers and one of the pair of second gate spacers opposing the one of the pair of first gate spacers, a first portion of the first interlayer insulating layer including an oxidized element semiconductor material.

35. The semiconductor device of claim **34**, wherein the first portion of the first interlayer insulating layer is an upper portion of the first interlayer insulating layer or a lower portion of the first interlayer insulating layer.

36. The semiconductor device of claim **34**, wherein the first portion of the first interlayer insulating layer is an entirety of the first interlayer insulating layer.

37. The semiconductor device of claim **34**, wherein the oxidized element semiconductor material includes at least one of germanium (Ge) or silicon (Si).

38. The semiconductor device of claim **34**, further including:

a third gate electrode on the substrate;

a fourth gate electrode on the substrate, the fourth gate electrode adjacent to and spaced apart from the third gate electrode;

a pair of third gate spacers at respective sides of the third gate electrode;

a pair of fourth gate spacers at respective sides of the fourth gate electrode;

a second interlayer insulating layer on the substrate, the second interlayer insulating layer between one of the pair of third gate spacers and one of the pair of fourth gate spacers opposing the one of the pair of third gate spacers.

39. The semiconductor device of claim **38**, wherein a first portion of the second interlayer insulating layer includes the oxidized element semiconductor material.

40. The semiconductor device of claim **39**, wherein an amount of the oxidized element semiconductor material included in the first portion of the first interlayer insulating layer is different from an amount of the oxidized element semiconductor material included in the first portion of the second interlayer insulating layer.

41. The semiconductor device of claim **39**, wherein a thickness of the first portion of the first interlayer insulating layer is different from a thickness of the first portion of the second interlayer insulating layer.

42. The semiconductor device of claim **38**, wherein the second interlayer insulating layer does not include the oxidized element semiconductor material.

43. The semiconductor device of claim **38**, wherein the second gate electrode and the third gate electrode are a same electrode provided between the first gate electrode and the fourth gate electrode.

44. The semiconductor device of claim **38**, wherein slopes of the first, second, third, and fourth gate spacers or slopes of sidewalls of the first, second, third, and fourth gate electrodes include both a positive sign and a negative sign.

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